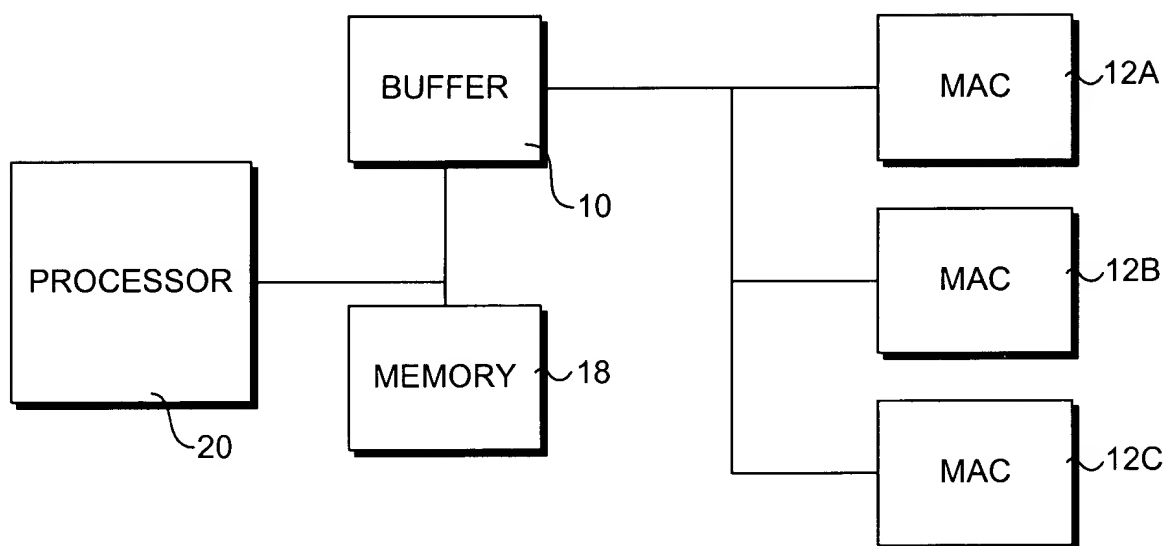
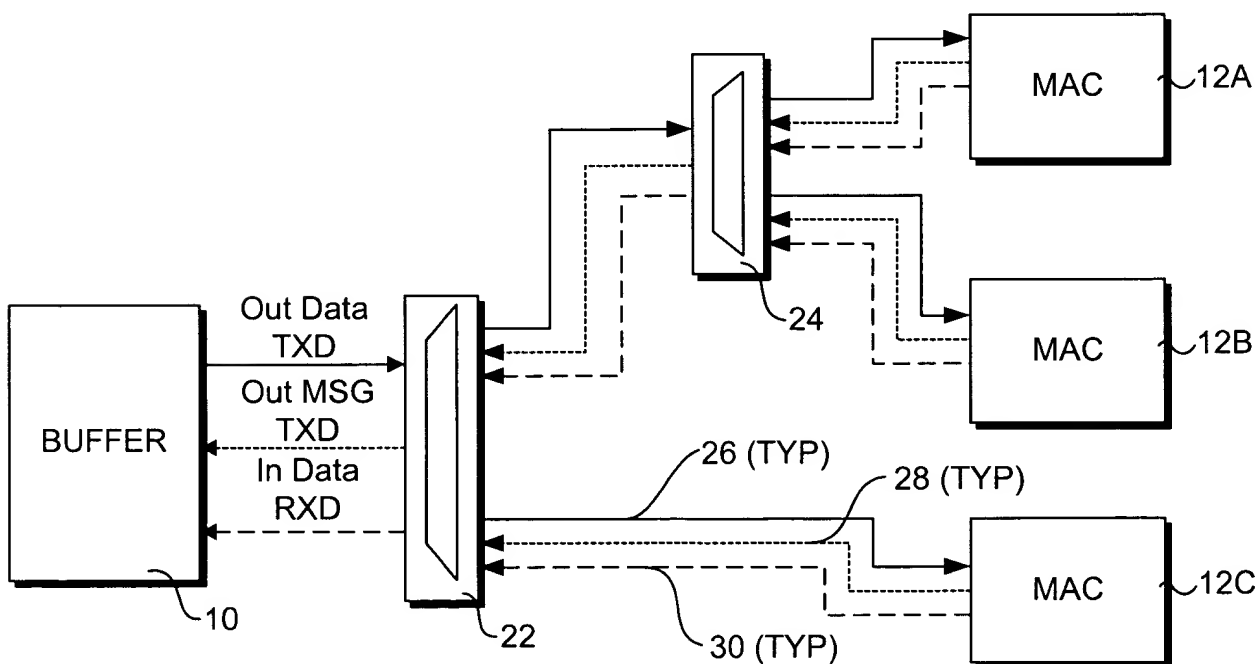


**FIG. 1**

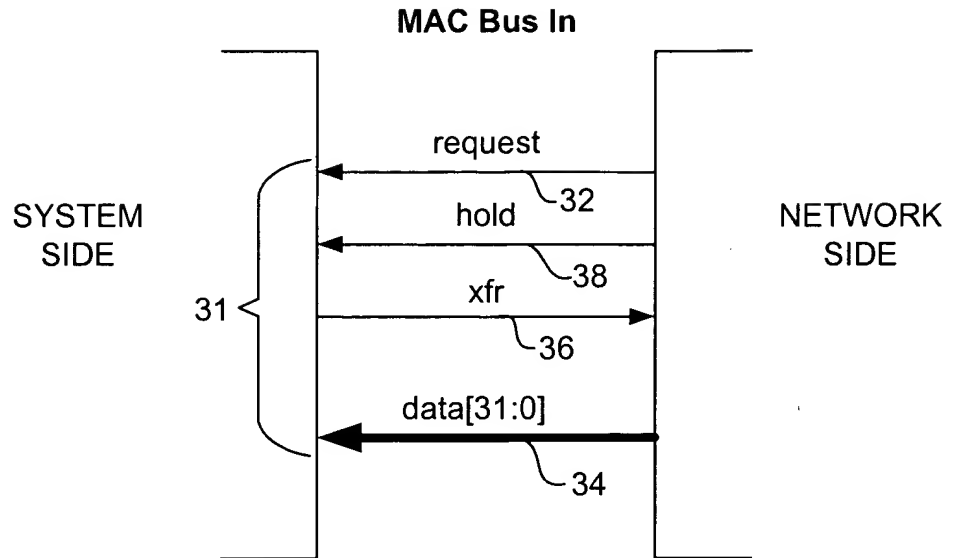


**FIG. 2**

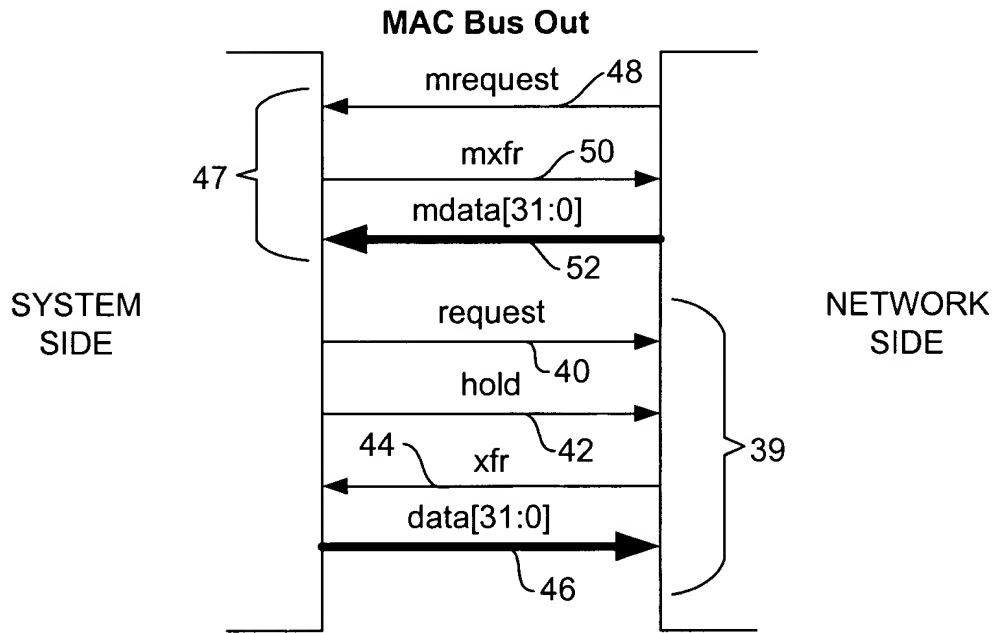


**FIG. 3**

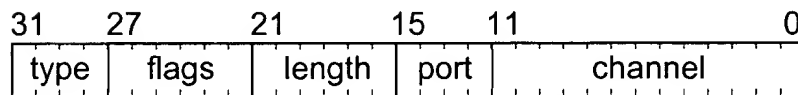
**FIG. 4**



**FIG. 5**

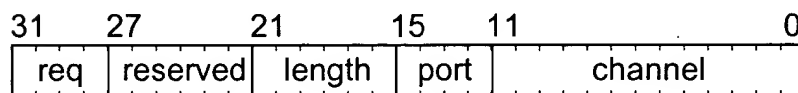


**DATA PACKET HEADER WORD**



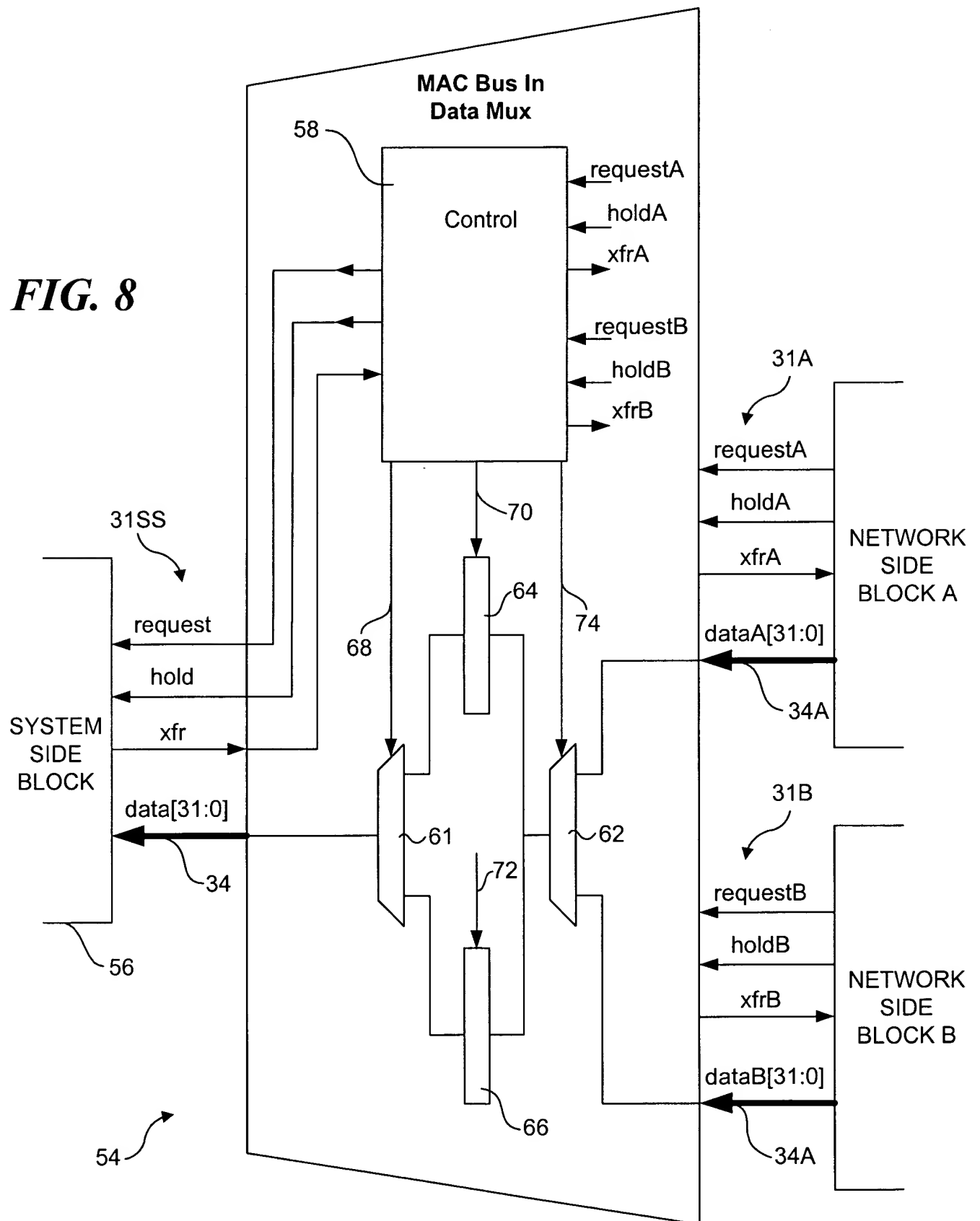
**FIG. 6**

**REQUEST MESSAGE WORD**

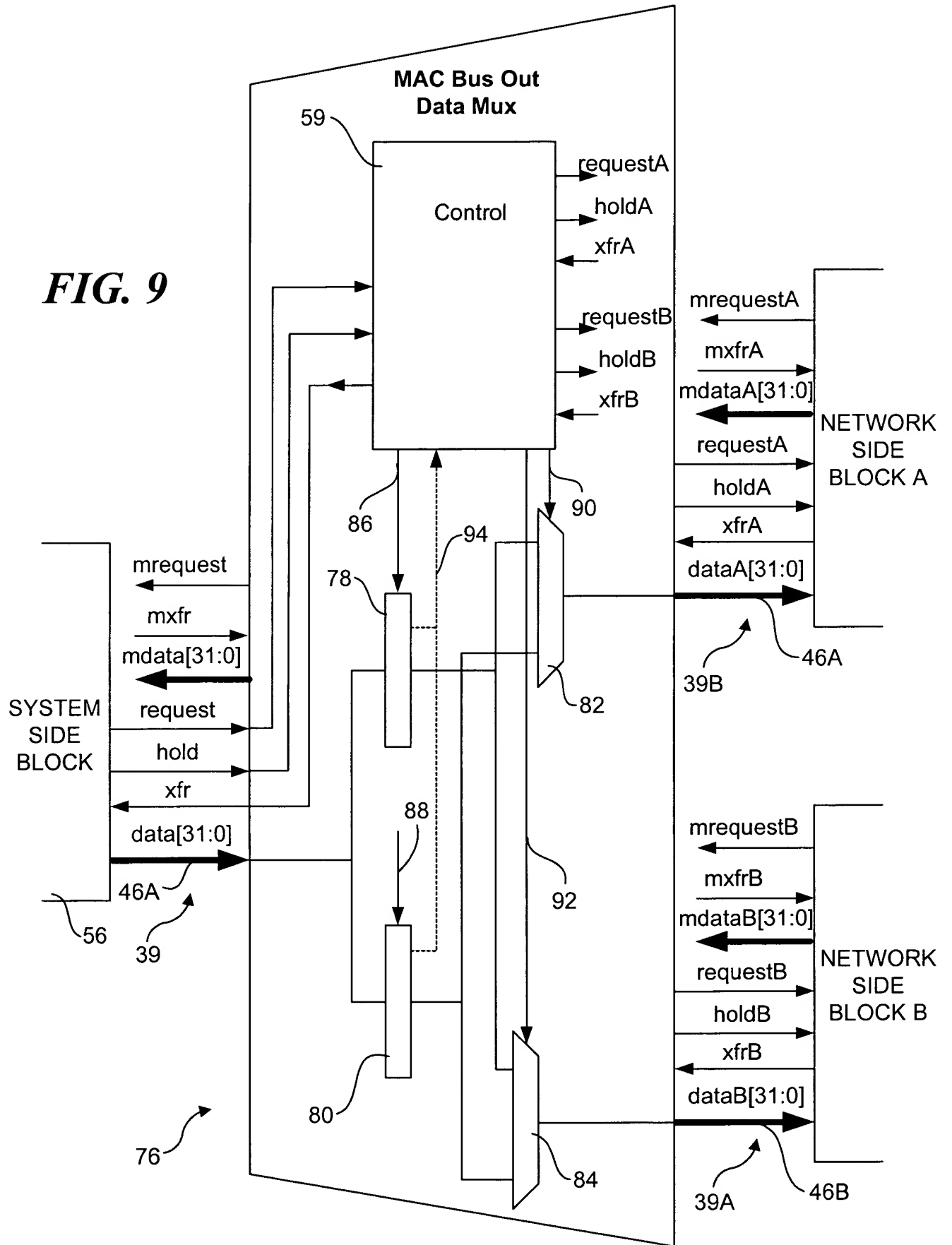


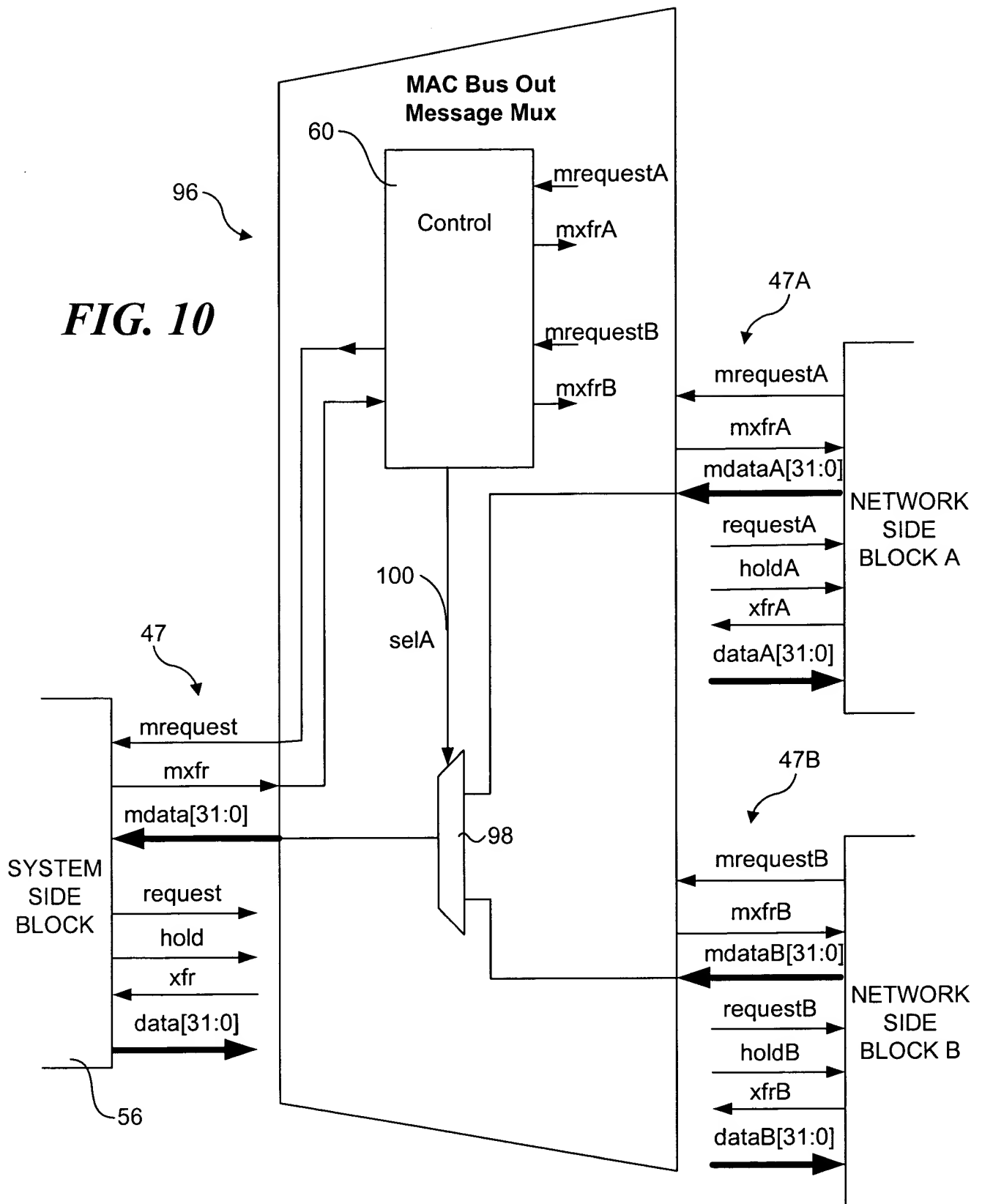
**FIG. 7**

**FIG. 8**



**FIG. 9**





register management flip-flops

inputis 1

reg1last

reg1full

data buffer registers

reg 1

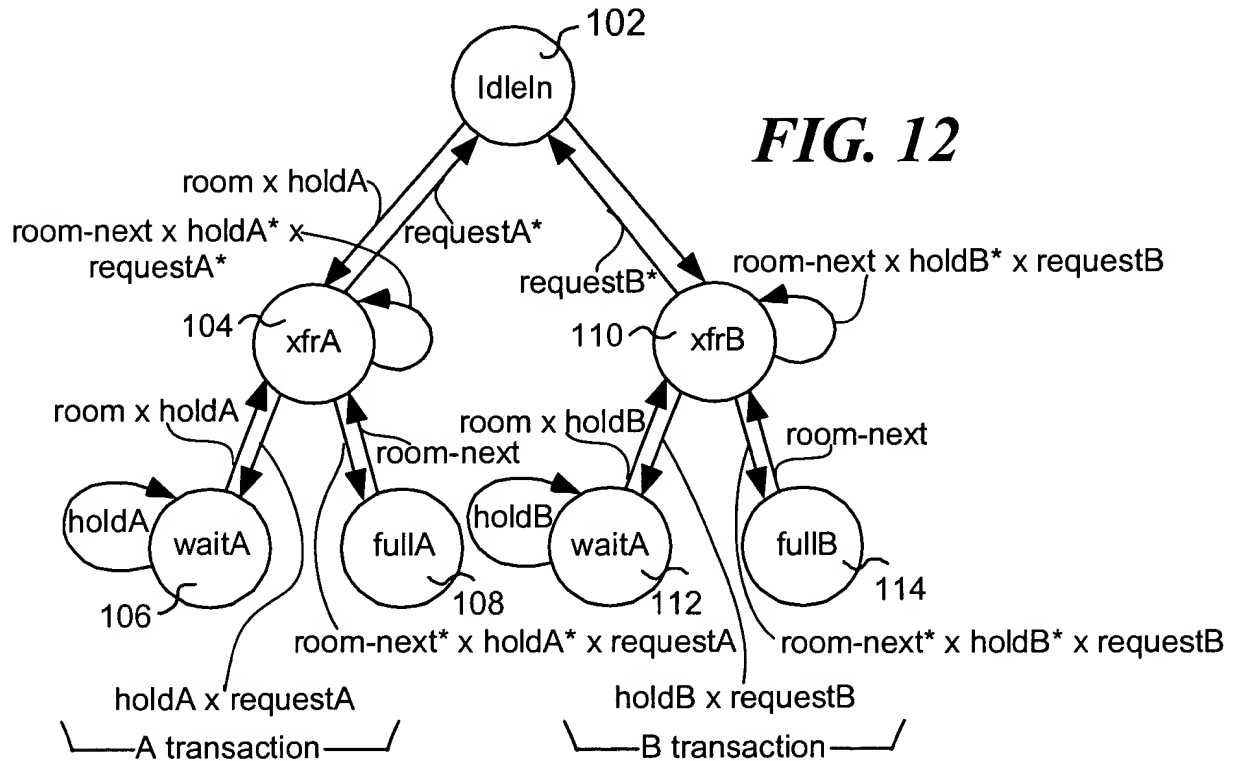
outputis 1

reg2last

reg1full

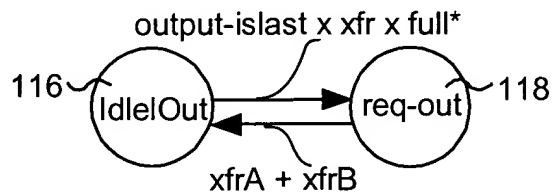
reg 1

**FIG. 11**



transaction = IdleIn\*  
 room-next = empty + xfr  
 room = reg1full\* + reg2full + xfr  
 full = reg1full x reg2full  
 empty = reg1full\* x reg2full\*

**FIG. 13**



register management flip-flops

inputis 1

route2A1

reg1last

reg1full

data buffer registers

reg 1

outputis 1

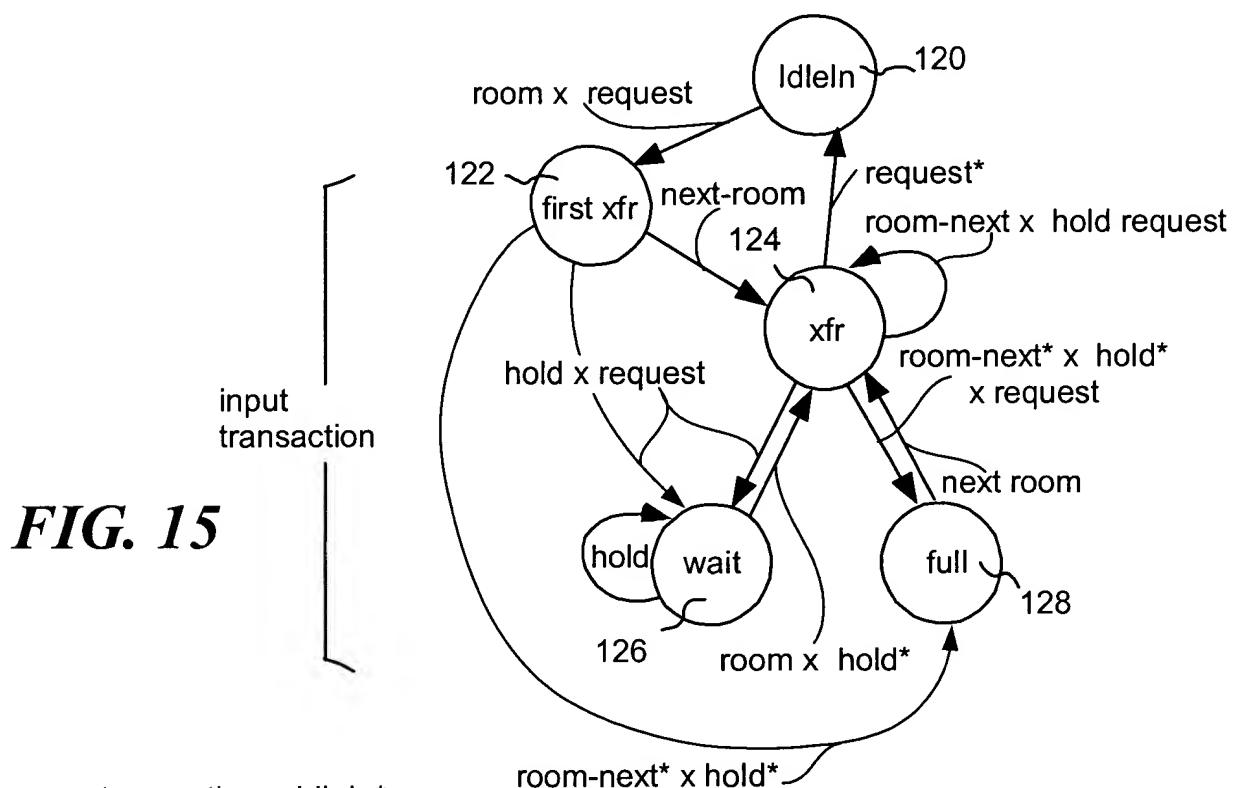
route2A2

reg2last

reg2full

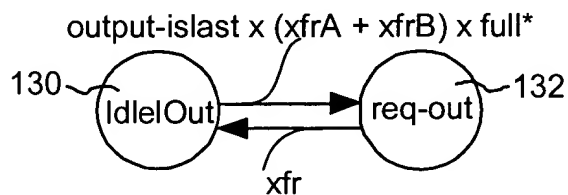
reg 1

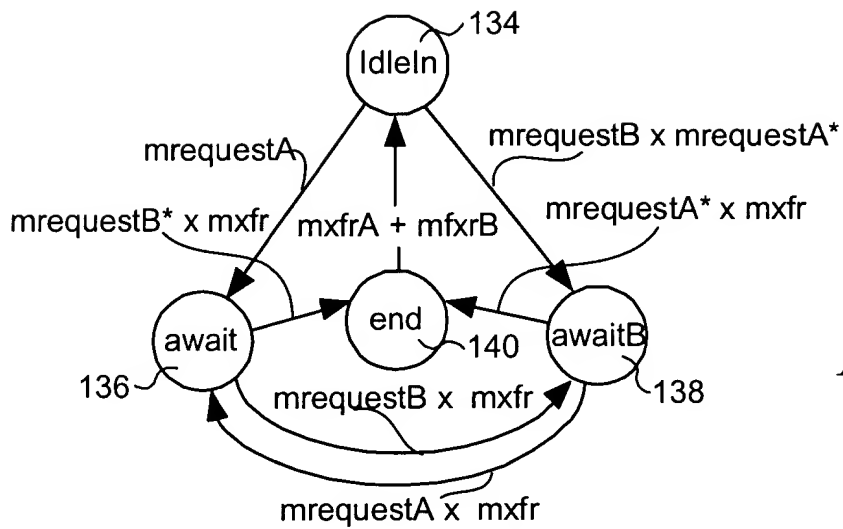
**FIG. 14**



transaction = IdleIn\*  
 room-next = empty + xfrA + xfrB  
 room = reg1full\* + reg2full\* + xfrA + xfrB  
 full = reg1full x reg2full  
 empty = reg1full\* x reg2full\*

**FIG. 16**

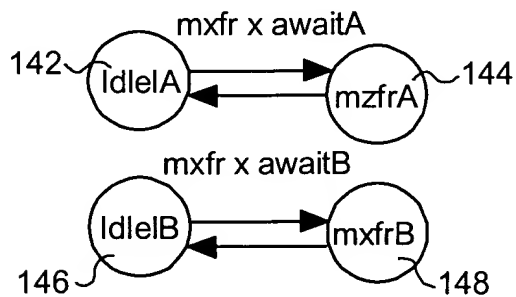




**FIG. 17**

Message transfers are one word long  
 merquest = awaitA = awaitB  
 selA = awaitA

mxfr machines for A and B network side input port



**FIG. 18**



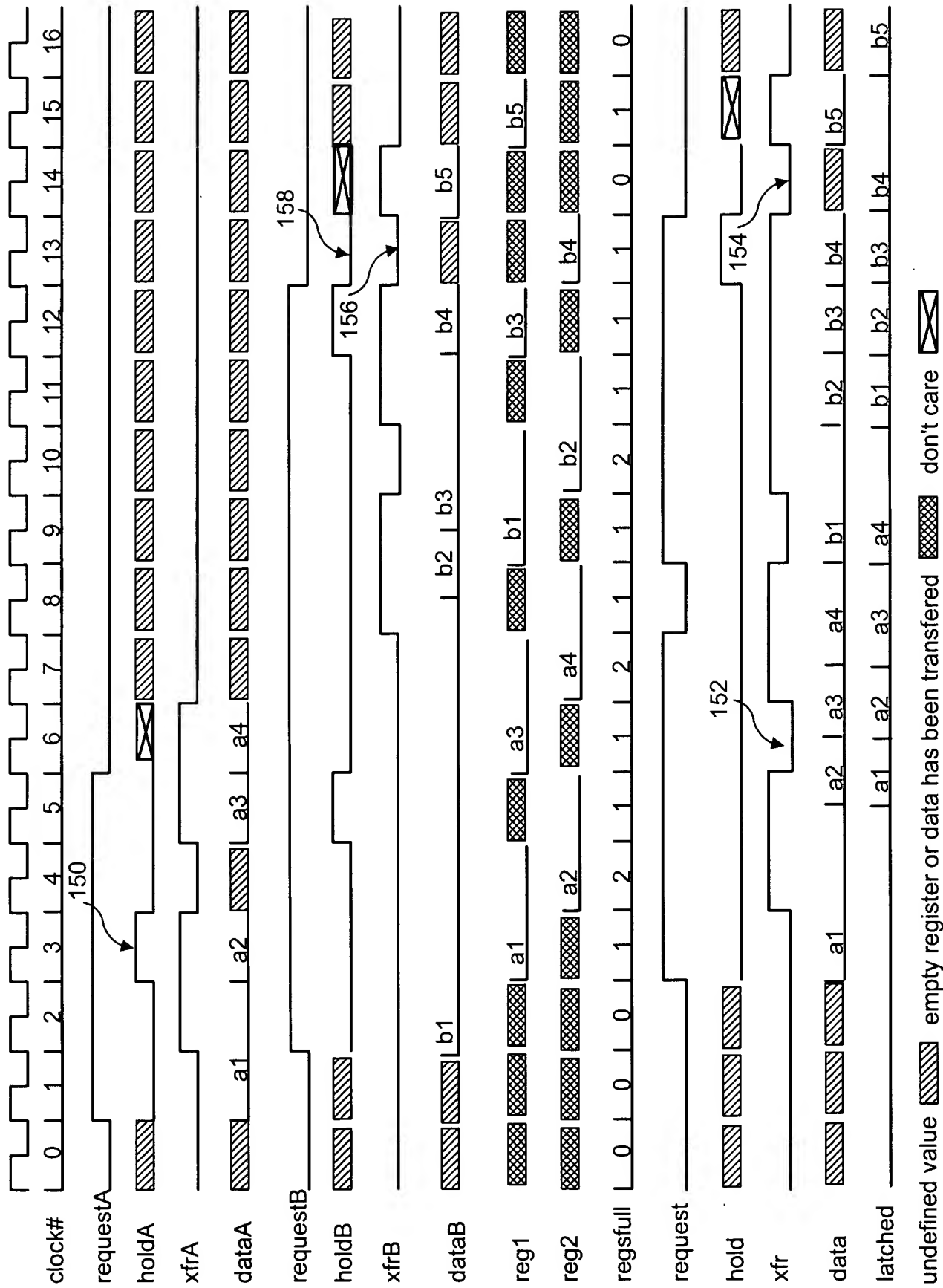


FIG. 19

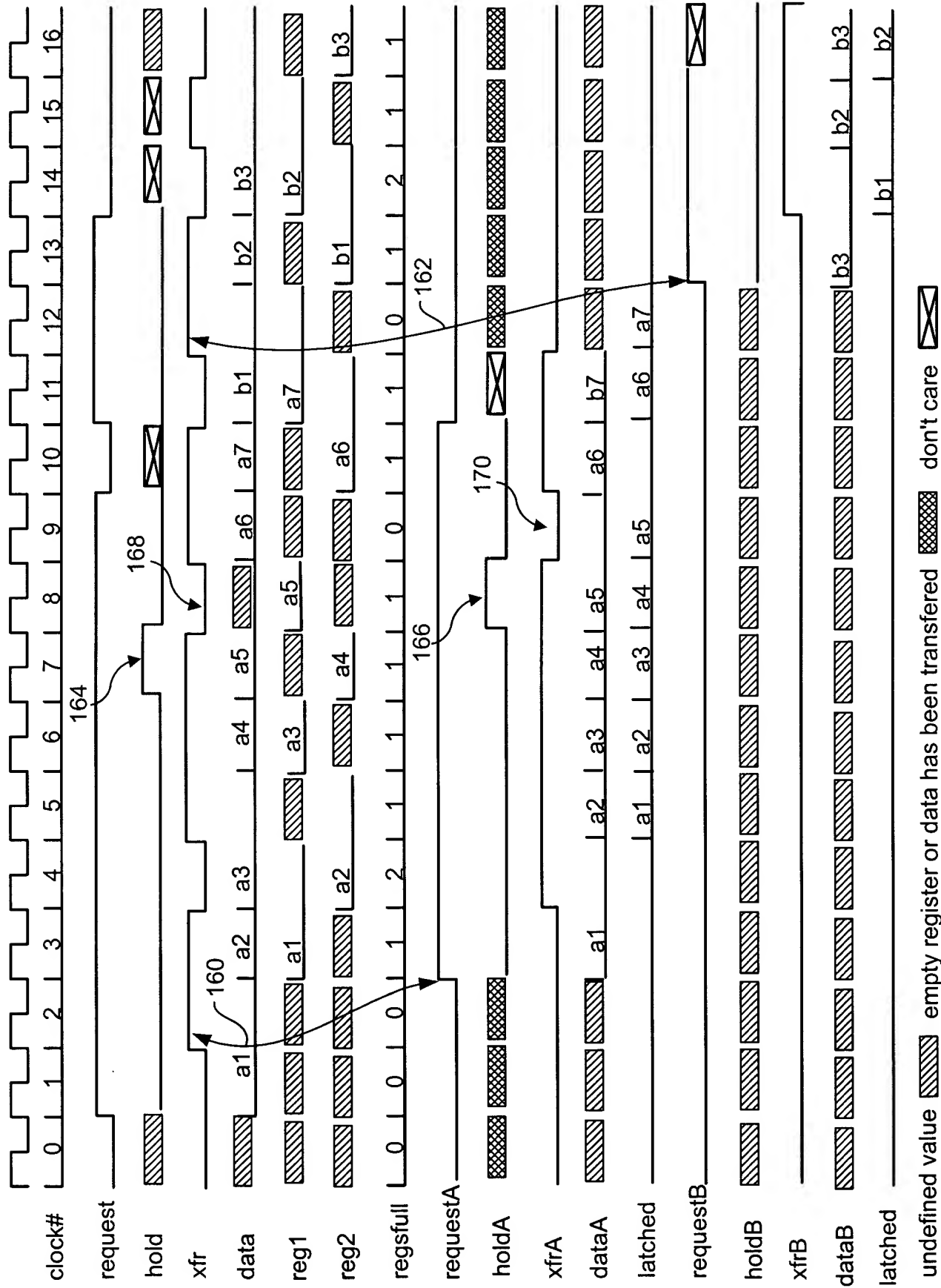


FIG. 20

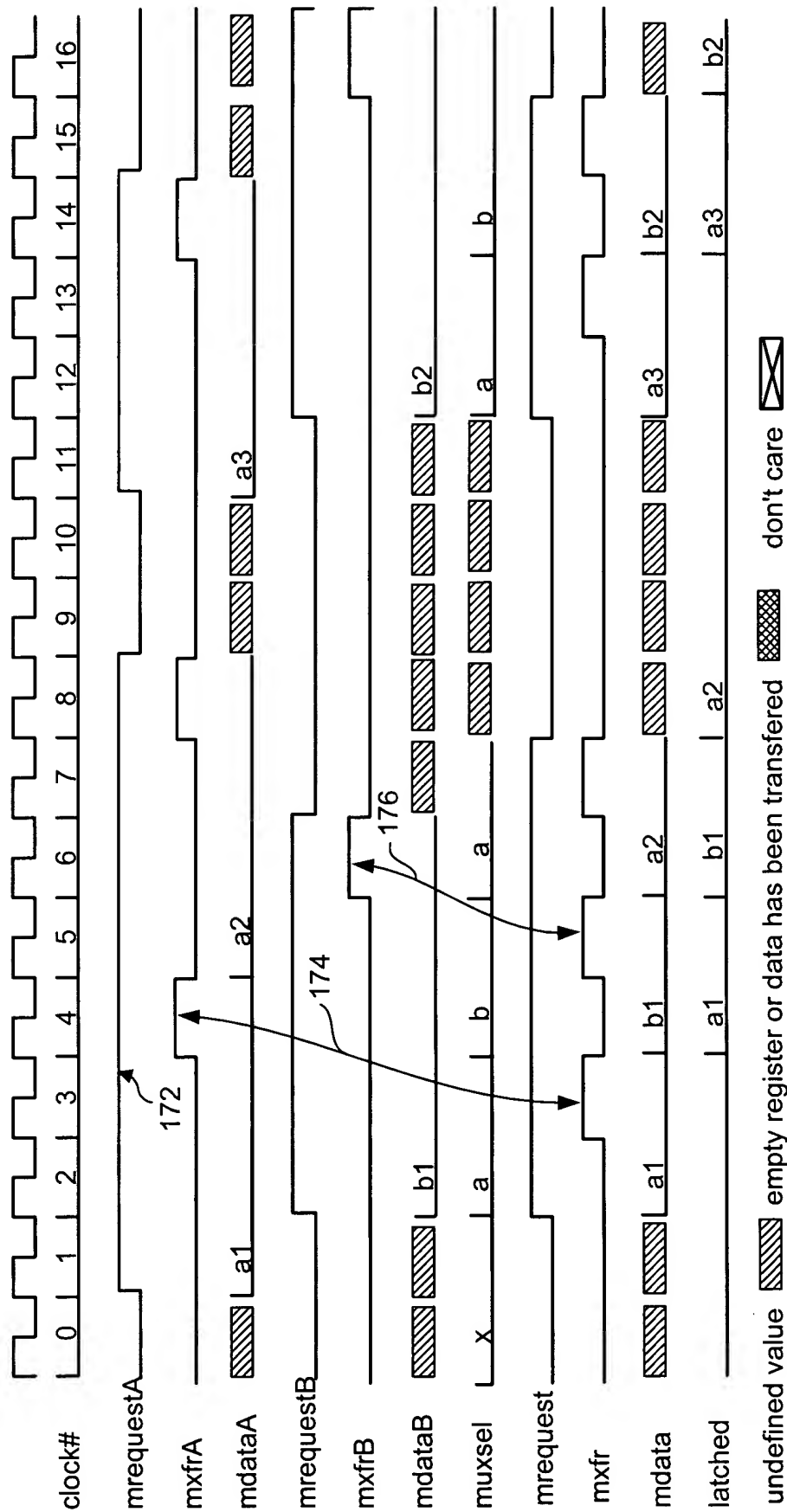


FIG. 21